

ABSTRACT OF THE DISCLOSURE

A method for fabricating a merged logic device is disclosed which simplifies the process by forming a deep junction of a double diffused drain (DDD) structure by a retrograded well ion implantation process. The method includes

- 5 forming a high voltage p-type well region on a semiconductor substrate;
simultaneously conducting an ion implantation for forming a logic p-type well region on a logic region and a high voltage n-type well region on the high voltage p-type well region; forming a high voltage gate oxide film on the entire surface and
conducting a threshold voltage ion implantation process; forming a logic gate oxide
- 10 film on the logic region and simultaneously forming a logic gate electrode and a high voltage gate electrode; forming a logic DDD region on the logic region and forming spacers on the sides of the gate electrodes; and forming logic source/drain regions, high voltage source/drain regions and a bulk bias control region.